REMARKS

The Office Action dated October 23, 2003 has been received and carefully noted. The above amendments to claims and the following remarks are submitted as a full and complete response thereto. Claims 1-12 are pending in this application. Claims 1, 2, 3 and 11 are amended. No new matter is presented. In the outstanding Office Action, claims 1-12 were rejected under 35 U.S.C. §103(a). In view of the above amendments and the following remarks, Applicant requests the favorable consideration of claims 1-12.

35 U.S.C. 103(a)

Claims 1-12 were rejected under 35 U.S.C. 103(a) as being unpatentable over Uchiyama et al. (U.S. Patent No. 5, 574,876) in view of Fadavi-Ardekani et al. (U.S. Patent No. 6,401,176). The Office Action takes the position that the combination of Uchiyama Fadavi-Ardekani teach and/or suggest all the features of the rejected claims. Applicants respectfully disagree.

Claim 1 recites a synchronous DRAM comprising, one memory array divided into a plurality of logical memory blocks, mode storage units so disposed in a plurality of stages as to correspond to the logical memory blocks, for storing control information for defining operation modes of the logical memory blocks. A setting unit is provided for setting the control information designated by a mode setting instruction to the mode storage unit corresponding to the logical memory block designated by the mode setting instruction in accordance with the mode setting instruction outputted from a plurality of controllers. A mode selection unit is provided for selecting the mode storage unit corresponding to the memory block containing a memory cell designated by an address inputted from one of the

controllers, and an access unit for executing an access operation in synchronism with a predetermined clock signal for the corresponding one of the logical memory blocks in accordance with the control information stored in the mode storage unit selected.

Uchiyama is directed to a main storage apparatus that is a synchronous dynamic memory having a plurality of memory banks, a node register, and a main storage controller. Uchiyama further discloses a memory having two memory banks and a mode register for determining an operation mode of the chip. Fadavi-Ardekani discloses the shared usage of a synchronous memory by a plurality of agents or processors. However, Fadavi-Ardekani does not cure the deficiencies of Uchiyama.

It is submitted that the combination of Uchiyama and Fadavi-Ardekani fail to teach and/or suggest a mode storage units so disposed in a plurality of states as to correspond to the logical memory blocks, for storing information for defining operation modes of the logical memory blocks. In other words, plurality of mode storage units that are disposed corresponding to each of the logical memory blocks.

In the claimed invention, however, each memory block is allowed to independently operate in the operation mode represented by the control information stored in the corresponding mode storage unit. As a result, the synchronous DRAM as recited enables a plurality of controllers requiring different operation modes to share the synchronous DRAM among them. Thus, the combination of Uchiyama and Fadavi-Ardekani fail to teach and/or suggest the feature of mode storage units so disposed in a plurality of stages as to correspond to the logical memory blocks, for storing control information for defining operation modes of the logical memory blocks. Accordingly, Applicants request the withdrawal of the rejection of claim 1 under 35 U.S.C. 103(a).

Claims 2-12 are dependent upon claim 1. It is submitted that claims 2-12 recite subject matter that is neither taught nor suggested by the applied reference for at least the reasons mentioned above. Therefore, Applicants request the withdrawal of the rejection of claims 2-12 under 35 U.S.C. 103(a).

The Office Action rejected claims 1, 2, and 4-12 under 35 U.S.C. § 103(a) over Usami (U.S. Patent No. 6,205,516B1) in view of Fadavi-Ardekani (U.S. Patent No. 6,401,176). The Office Action took the position that the combination of the cited references teach or suggest all the features recited in claims 1, 2, and 4-12. Applicants respectfully disagree.

Usami discloses a method for designating a unique address data to select mode operations via mode register 35. A memory control circuit 5a is utilized to control the ROM 2, the internal RAM 3, and the extended RAM 4. The internal RAM 3 is constructed from 8 SDRAMS. RAM 3 and RAM 4 are physically separated from each other, and each has a predetermined capacity.

In contrast, the memory array of the present invention is divided into a plurality of logical memory blocks. As a result, the capacity of each logical memory block of the invention can be set to an optional value. Therefore, the SDRAM of the invention can deal with various accesses from a plurality of controllers.

Thus, Usami neither teaches nor suggests the feature of changing the operation modes in one SDRAM as recited in the claimed invention. Thus, Usami fails to teach or suggest a synchronous DRAM comprising a setting unit for setting the control information designated by a mode setting instruction to the mode storage unit corresponding to the logical memory block designated by the mode setting instruction in accordance with the

mode setting instruction outputted from a plurality of controllers. Furthermore, Usami fails to teach or suggest a mode selection unit for selecting the mode storage unit corresponding to the logical memory block containing a memory cell designated by an address inputted from one of the controllers. In addition, as admitted in the Office Action, Usami fails to teach that the programmable registers are programmed via instructions outputted from a plurality of controllers.

Fadavi-Ardekani fails to cure the deficiencies of Usami. As a result, Applicants respectfully submit that applied references neither teach nor suggest the features recited in claim 1. Therefore, Applicants request the withdrawal of the rejection of claim 1 under 35 U.S.C. 103(a).

Claims 2, and 4-12 are dependent upon independent claim 1. Therefore, claims 2, and 4-12, for at least the reasons mentioned above, recite subject matter that is neither taught nor suggested by the applied references. Applicants respectfully request the withdrawal of the rejection of claims 2 and 4-12 under 35 U.S.C. 103(a).

Claims 1-12 were rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Rao (U.S. Patent No. 6, 173,356 B1) in view of Usami. The Office Action takes the position that the combination of Rao and Usami teach and/or suggest the features recited in claims 1-12. Applicants respectfully disagree.

Rao discloses a multiprocessor that includes a memory system having a memory controller for linking a plurality of processors with an integrated memory. Rao also discloses mode registers 415 that used for setting optional access modes such at the page reads and writes or burst access with a selected burst type.

As discussed above, Usami fails to teach and/or suggest Usami neither teaches nor

suggests the feature of changing the operation modes in one SDRAM as recited in the claimed invention. Thus, Usami fails to teach or suggest a synchronous DRAM comprising mode storage units so disposed in a plurality of stage as to correspond the logical memory blocks, for storing control information for defining operation modes and the logical memory blocks. Furthermore, Usami fails to teach or suggest a mode selection unit for selecting the mode storage unit corresponding to the logical memory block containing a memory cell designated by an address inputted from one of the controllers.

Thus, Usami fails to teach and/or suggest the deficiencies of Rao. As a result, Applicants respectfully submit that claim 1 recites subject matter this patentable. Therefore, Applicants request the withdrawal of the rejection of claim 1 under 35 U.S.C. 103(a).

Claims 2-12 depend upon independent claim 1, therefore it is submitted that these claims, for at least the reasons mentioned above, likewise recite subject matter that is neither taught nor suggested by the applied references. As a result, Applicants request the withdrawal of the rejection of claims 2-12 under 35 U.S.C. 103(a).

Claims 1-12 were rejected under 35 U.S.C. 103(a) as being unpatentable over Farrer (U.S. Patent 5, 307, 320) in view of Fadavi-Ardekani (U.S. Patent 6,401,176). The Office Action the position that the combination of Farrer and Fadavi-Ardekani disclose all the features recited in claims 1-10 and 12. Applicants respectfully disagree.

Farrer is directed to a memory controller for a dynamic random access memory. The memory controller includes multiple programmable storage registers, where one register is associated with every bank location in the memory array. More specifically, Farrer discloses that each programmable register is independently programmed to contain

access parameters that are necessary to access its associated bank. Thus, Farrer merely discloses a memory controller that can be adaptive to various types of DRAM banks by associating programmable storage registers with each DRAM bank. However, Farrer fails to disclose a synchronous DRAM or that the programmable registers are programmed via instructions outputted from a plurality of controllers. The Office Action takes the position that Fadavi-Ardekani discloses the deficiencies of Farrer. Applicants respectfully disagree.

Fadavi-Ardekani discloses the shared usage of a synchronous memory by a plurality of agents or processors. However, Fadavi-Ardekani fails to cure the deficiencies of Farrer. In particular, the applied reference fail to teach or suggest a synchronous DRAM comprising a setting unit, a mode selection unit, and an access unit as recited in the claimed invention. More specifically, the applied references do not teach or suggest an SDRAM having multiple mode registers so as to perform the independent operations in different operation modes in the single SDRAM.

The applied references either alone or in combination fail to teach or suggest a synchronous DRAM having mode storage units so disposed in a plurality of stages as to correspond to the logical memory blocks, for storing control information for defining operation modes of the logical memory blocks. The applied references also fail to teach or suggest a mode selection unit for selecting the mode storage unit corresponding to the memory block containing a memory cell designated by an address inputted from one of the controllers. Thus, Applicants request the withdrawal of the rejection of claim 1 under 35 U.S.C. 103(a).

Claims 2-12 depend upon independent claim 1, therefore it is submitted that these claims, for at least the reasons mentioned above, likewise recite subject matter that is

neither taught nor suggested by the applied references. As a result, Applicants request the withdrawal of the rejection of claims 2- 12 under 35 U.S.C. 103(a).

Conclusion

Applicant's amendments and remarks have overcome the rejections set forth in the Office Action dated October 23, 2004. Applicant's remarks have distinguished claims 1-12 and thus overcome the rejection of these claims under 35 U.S.C. §103(a). Claims 1, 2, 3, and 11 have been amended. No new matter is presented. Accordingly, in view of the above remarks and amendments claims 1-12 are in condition for allowance. Therefore, Applicant respectfully requests consideration and allowance of claims 1-12.

Should the Examiner believe anything further is desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact Applicants' undersigned attorney at the telephone number listed below.

In the event this paper is not considered to be timely filed, Applicants respectfully petition for an appropriate extension of time. The Commissioner is authorized to charge payment for any additional fees which may be required with respect to this paper to Counsel's Deposit Account 01-2300, referring to client-matter number 100021-00046.

Respectfully submitted,

Arent Fox Kintner Plotkin & Kahn

Bala K. Sundararajan
Attorney for Applicants
Reg. No. 50,900

Customer No. 004372
1050 Connecticut Ave. NW
Suite 400
Washington, D.C. 20036-5339
Tel: (202) 857-6261
Fax: (202) 638-4810
BKS